REMARKS

In section 2 of the Office Action, the Examiner objected to claim 21. Claim 21 has accordingly been amended to overcome the objection.

In section 3 of the Office Action, the Examiner rejected claims 32-40 under 35 U.S.C. §103(a) as being unpatentable over the Chiang patent in view of the Litwin patent.

The Chiang patent discloses a varactor 31 in Figure 1. The varactor 31 has an active semiconductor layer 32 which is sandwiched between a dielectric film 33 and an n-type ground electrode 34. A gate electrode 35 is deposited on top of the dielectric film 33. The varactor 31 is supported on an insulating substrate 36.

The varactor 31 is switched back and forth between its maximum capacitance accumulation mode and its minimum capacitance depletion mode by reversing the polarity of its gate voltage Vg. Whenever the gate 35 of the varactor 31 is positively biased, electrons are accumulated in the silicon layer 32 near its interface with the dielectric film 33. Conversely, when the gate 35 is sufficiently negatively biased, the silicon layer 32 is depleted of electrons.

The Chiang patent states that, if the active silicon layer 32 is single crystal silicon, capacitive switching ratios R well in excess of two can be achieved. However, according to the Chiang patent, existing single crystal silicon technology is not applicable to the fabrication of large area integrated circuits, and it is difficult to obtain high capacitive switching ratios R for the varactor 31 if its active semiconductor layer 32 is composed of amorphous silicon.

The Chiang patent also discloses a varactor 41 in Figures 2 and 3. The varactor 41 has smaller effective capacitive surface areas in depletion than in accumulation, and the varactor 41 uses poly-silicon thin films. The varactor 41 has a ground layer 42 of undoped or very lightly doped silicon on a thick insulating substrate 43. A thin dielectric film 44 is formed on the ground layer 42, and a metal or silicon p+ or n+ gate electrode 46 is deposited on the dielectric film 44.

N-type or p-type ground electrodes 45 are configured so that they only partially and laterally overlap the gate electrode 46. As a result, the gate electrode 46 longitudinally aligns with a section 47 of the active silicon layer 42 which is beyond the lateral margins of the ground electrodes 45, but which is in

intimate electrical contact with the substrate 43. The extent to which the ground electrodes 45 laterally overlap the gate electrode 46 is determined by the lateral scattering of impurities during doping of the ground electrodes 45 as the impurities migrate into the silicon film 42.

The Chiang patent states that the capacitive switching ratio R for the varactor 41 is controlled by the ground-gate overlap. In other words, the capacitive switching ratio R for the varactor 41 is equal to the ratio of the length L of the gate to the ground overlap length $2L_2$. The Chiang patent further states that there is a performance tradeoff between switching speed and RF impedance on the one hand and capacitive switching ratio R on the other. Thus, switching speed can be increased and RF impedance can be lowered at the cost of decreased capacitive switching ratio R. Alternatively, the capacitive switching ratio R can be increased at the cost of decreased switching speed and increased RF impedance.

A varactor 51 as shown in Figure 4 is a bottom-gate counterpart to the varactor 41.

Figures 5 and 6 show top-gate and bottom-gate varactors 61 and 62, respectively. The ground electrodes 45 of the varactors 61 and 62 reside in a suitably

patterned conductive layer 63 which is physically distinct from the active silicon film 42, but which is in intimate contact therewith in partially overlapping alignment with the gate electrode 46. Again, the capacitive switching ratios R for the varactors 61 and 62 are controlled by their respective ground-gate overlaps.

A top-gate varactor 71 shown in Figures 7 and 8 has gate electrode segments 46a-46m and ground electrode segments 45a-45n which are laterally staggered with respect to the gate electrode segments 46a-46n, where n = m + 1. Each of the gate electrode segments 46a-46m is partially and laterally overlapped by two of the ground electrode segments 46a-46n such that neighboring gate electrode segments share the ground electrode segments that are disposed between them. Accordingly, each of the intermediate ground electrode segments partially overlaps the gate electrode segments to its immediate right and left. The gate electrode segments 46a-46m are electrically interconnected, and the ground electrode segments 45a-45n are electrically interconnected.

Figure 9 illustrates a varactor 81 which is a bottom-gate counterpart to the varactor 71.

Independent claim 32 - The Examiner recognizes that the Chiang patent does not disclose a varactor

having a plurality of alternating P- type wells and N+ type regions in a silicon layer. Therefore, the Examiner relies on Figure 2 of the Litwin patent which shows a varactor 20 having n+ type source and drain regions and a p type well. The Examiner then argues that, because lightly doped well regions are desirable as evidenced by the Litwin patent, it would have been obvious to incorporate such lightly doped well regions in the varactors disclosed in the Chiang patent to form varactors having a plurality of alternating P- type wells and N+ type regions in a silicon layer.

However, there are a number of problems with this argument. First, it is assumed that the Examiner intends for the silicon layer 42 of the Chiang patent to read on the silicon layer recited in independent claim 32. In this case, the Chiang patent discloses that silicon layer is undoped or very lightly doped but does not disclose the type of doping. The Chiang patent also discloses that the silicon layer 42 is degenerately doped with n- type or p- type impurities to form the ground electrodes 45. However, the Chiang patent does not disclose such doping forms N+ regions alternating with P- type wells.

Therefore, even if the p type silicon layer 22 is used for the silicon layer 42, a varactor having a silicon layer with alternating P- type wells and N+ type regions does not result.

Accordingly, for this first reason, independent claim 32 is not obvious over the Chiang patent in view of the Litwin patent.

Second, the Examiner may choose to argue that Figure 2 of the Litwin patent suggests doping the silicon layer 42 with p type and n+ type impurities according to the silicon layer 22 and regions 23 and 24 disclosed in the Litwin patent. If such doping is assumed, then the region 47 will be a p type region, and the ground electrodes 45 will be n+ type ground electrodes.

As can be seen, a varactor having a silicon layer with alternating P- type wells and N+ type regions still does not result.

Accordingly, for this second reason, independent claim 32 is still not obvious over the Chiang patent in view of the Litwin patent.

Third, the Chiang patent disclose that the capacitive switching ratio R of its varactor is dependent on the gate-ground overlap ratio. Thus, the Chiang patent discloses that the capacitive switching ratio R

can be increased by increasing gate length versus ground overlap length.

On the other hand, the Litwin patent discloses that the capacitive switching ratio R (referred to in the Litwin patent as dynamic range) of its varactor can be made high by making the well as lightly doped as possible. Indeed, the Litwin patent discloses that doping of the well should be blocked. (See column 5, lines 36-40 of the Litwin patent.)

Accordingly, the Litwin patent suggests that the region 47 of the silicon layer 42 disclosed in the Chiang patent should not be doped. Therefore, the region 47 will not be N+, N-, P+, or P-.

Consequently, the Litwin patent does not suggest processing of the varactors disclosed in the Chiang patent so that the varactor of independent claim 32 results.

Therefore, for this third reason, independent claim 32 is not obvious over the Chiang patent in view of the Litwin patent.

Fourth, the Chiang patent and the Litwin patents disclose controlling the capacitive switching ratios of their varactors by such different mechanisms

that neither suggests a combination that results in the varactor of independent claim 32.

Therefore, for this fourth reason, independent claim 32 is not obvious over the Chiang patent in view of the Litwin patent.

Because independent claim 32 is patentable over the Chiang patent in view of the Litwin patent, dependent claims 33-40 are similarly patentable over the Chiang patent in view of the Litwin patent.

Moreover, dependent claim 34 requires the SOI structure recited in independent claim 32 to include a layer of high resistivity silicon under the insulation layer. The Litwin patent does not disclose an SOI structure, and the Chiang patent does not disclose that the insulating layer 43 is over a silicon layer or that such a silicon layer is high resistivity silicon. Accordingly, the combination of the Chiang patent and the Litwin patent does not disclose or suggest the invention of dependent claim 34.

The Examiner contends that it is well known that silicon handle layers below the insulating layers of SOI structures are highly resistive. However, the Examiner has cited no art to support this contention or to support an argument that the use of a high resistivity

silicon handle layer is obvious with respect to the varactor of dependent claim 34.

Therefore, dependent claim 34 is not obvious over the Chiang patent in view of the Litwin patent.

Dependent claim 37 recites that the P- wells form a transistor body, and that the transistor body is allowed to float. Neither the Chiang patent nor the Litwin patent discloses or suggests this feature. Accordingly, the combination of the Chiang patent and the Litwin patent does not disclose or suggest the invention of dependent claim 37.

The Examiner makes no contentions or arguments with respect to dependent claim 37.

Therefore, dependent claim 37 is not obvious over the Chiang patent in view of the Litwin patent.

Dependent claim 39 recites that the capacitive switching ratio is equal to or greater than 5. The only capacitive switching ratio mentioned in the Chiang patent is greater than 2, and the Litwin patent does not mention any specific capacitive switching ratios.

Moreover, the Examiner argues that a high capacitive switching ratio is desirable. However, neither the Chiang patent nor the Litwin patent disclose

how to achieve a capacitive switching ratio equal to or greater than 5.

Therefore, dependent claim 39 is not obvious over the Chiang patent in view of the Litwin patent.

Dependent claim 40 recites that the capacitive switching ratio is equal to or greater than 20. The only capacitive switching ratio mentioned in the Chiang patent is greater than 2, and the Litwin patent does not mention any specific capacitive switching ratios.

Moreover, the Examiner argues that a high capacitive switching ratio is desirable. However, neither the Chiang patent nor the Litwin patent disclose how to achieve a capacitive switching ratio equal to or greater than 20.

Therefore, dependent claim 40 is not obvious over the Chiang patent in view of the Litwin patent.

CONCLUSION

In view of the above, the claims of the present application are definite and patentably distinguish over the art applied by the Examiner. Accordingly, allowance of these claims and issuance of the present application are respectfully requested.

Respectfully submitted,

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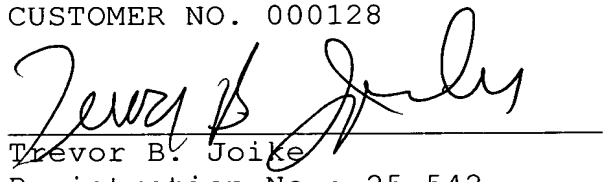
By: 

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